What is claimed is:

1. A digital bus comprising:

a transmitter unit capable of generating a plurality of clock signals;

a receiver unit comprising:

one or more first-in-first-out (FIFO) units; and

a synchronizer unit coupled to the one or more FIFO units, the synchronizer unit adapted to receive the plurality of clock signals, a sample clock signal, and a reset signal and to generate a plurality of write reset signals and a read reset signal, wherein each of the plurality of write reset signals has a latency with respect to the read reset signal of less than or equal to one clock cycle; and

a transmission medium to couple the plurality of clock signals from the transmitter unit to the receiver unit.

2. The digital bus of claim 1, wherein the transmitter unit comprises a transceiver.

3. The digital bus of claim 2, wherein the transceiver comprises a processor.

4. The digital bus of claim 1, wherein each of the plurality of clock signals comprises a pair of complementary clock signals.

5. The digital bus of claim 4, wherein the pair of complementary clock signals have a skew of less than 90 degrees.

6. The digital bus of claim 4, wherein each of the plurality of clock signals has a frequency of between about 500 megahertz and about five gigahertz.

7. The digital bus of claim 1, wherein the transmission medium comprises a cable.

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8. The digital bus of claim 1, wherein each of the plurality of clock signals has a clock frequency and the sample clock has a sample clock frequency that is about twice the clock frequency.

9. The digital bus of claim 1, wherein the transmission medium comprises a plurality of metal interconnects formed on a substrate.

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10. The digital bus of claim 1, wherein the transmission medium comprises free space.

11. The digital bus of claim 1, wherein the receiver unit comprises a memory unit.

12. The digital bus of claim 11, wherein the memory unit comprises a dynamic random access memory.

13. An integrated circuit comprising:

a transmitter unit capable of generating a plurality of clock signals;

a receiver unit comprising:

one or more first-in-first-out (FIFO) units; and

a synchronizer unit coupled to the one or more FIFO units, the synchronizer unit adapted to receive the plurality of clock signals and a sample clock signal and to generate a plurality of write reset signals and a read reset signal, wherein each of the plurality of write reset signals has a latency with respect to the read reset signal of less than or equal to one clock cycle; and

a transmission medium to couple the plurality of clock signals from the transmitter unit to the receiver unit.

14. The integrated circuit of claim 13, wherein the transmitter unit, the receiver unit, and the transmission medium are fabricated on a single substrate.

15. The integrated circuit of claim 14, wherein the single substrate is silicon.

16. The integrated circuit of claim 13, wherein the transmission medium comprises a plurality of copper interconnects.

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17. The integrated circuit of claim 13, wherein the transmitter unit comprises a memory unit.

18. The integrated circuit of claim 17, wherein the memory unit comprises a dynamic random access memory.

19. The integrated circuit of claim 17, wherein the memory unit comprises a static random access memory.

20. A synchronizer unit comprising:

a logic circuit adapted to receive a plurality of clock signals, a reset signal, and a sample clock signal and to generate a synchronized reset signal synchronized to the reset signal, a plurality of write reset signals, and a read reset signal synchronized to the plurality of write reset signals, the read reset signal having a latency with respect to each of the plurality of write reset signals of less than or equal to one clock cycle.

21. The synchronizer unit of claim 20, wherein the logic circuit comprises complementary metal-oxide semiconductor logic circuits.

22. The synchronizer unit of claim 21, wherein the logic circuit comprises a plurality logic gates having a delay of less than about two nanoseconds.

23. A synchronizer unit comprising:

a first synchronizer unit to receive a plurality of clock signals and a reset signal and to generate a synchronized reset signal;

a second synchronizer unit to receive the plurality of clock signals and the synchronized reset signal and to generate a plurality of write reset signals; and

a third synchronizer unit to receive a sample clock signal, the synchronized reset signal, and the plurality of write reset signals and to generate a read reset signal having a latency with respect to each of the write reset signals of less than or equal to one clock cycle.

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24. The synchronizer unit of claim 23, wherein the first synchronizer unit comprises a plurality of clock signal paths, wherein each of the plurality of clock signal paths comprises a plurality of serially connected flip-flops.

25. The synchronizer unit of claim 24, further comprising an OR gate coupled to each of the plurality of clock signal paths, the OR gate having an output node providing the synchronized reset signal.

26. The synchronizer unit of claim 24, wherein the second synchronizer unit comprises a plurality of clock signal paths, wherein each of the plurality of clock signal paths comprises a plurality of serially connected flip-flops.

27. A method of forming a read reset signal, the method comprising:

synchronizing a first reset signal to a plurality of clock signals to form a synchronized reset signal;

synchronizing the synchronized reset signal to the plurality of clock signals to form a plurality of write reset signals; and

synchronizing the synchronized reset signal to a sample clock signal to form a read reset signal having a latency with respect to each of the plurality of write reset signals of less than or equal to one clock cycle.

28. The method of claim 27, wherein synchronizing a first reset signal to a plurality of clock signals to form a synchronized reset signal comprises:

clocking the first reset signal into a plurality of parallel flip-flops using the plurality of clock signals to clock each of the plurality of parallel flip-flops to form a plurality of clocked reset signals; and

ORing the plurality of clocked reset signals to form the synchronized reset signal.

29. The method of claim 27, wherein synchronizing the synchronized reset signal to the plurality of clock signals to form a plurality of write reset signals comprises:

clocking the synchronized reset signal into a plurality of parallel flip-flops using the plurality of clock signals to clock each of the plurality of parallel flip-flops to form the plurality of write reset signals.

30. The method of claim 27, wherein synchronizing the synchronized reset signal to a sample clock signal to form a read reset signal having a latency with respect to each of the plurality of write reset signals of less than or equal to one clock cycle comprises:

adjusting a number of flip-flops in a signal path such that the read reset signal with respect to each of the plurality of write signals has a latency of less than or equal to one clock cycle.